CLAIMS

1. A port independent data transaction interface for multi-port devices, comprising:

a command channel that receives command data and a source id, the source id indicating a source device that transmitted the command data;

a data-in channel that receives write data and a write source id, the write source id indicating a source device that transmitted the write data; and

a data-out channel that provides read data and a read id, the read id indicating a source device that transmitted a read command corresponding to the read data.

2. A port independent data transaction interface as recited in claim 1, wherein the source id is utilized to associate command data with corresponding write data.

3. A port independent data transaction interface as recited in claim 2, wherein the write data transmitted to the data-in channel and corresponding command data transmitted to he command channel are processed when transmitted during different clock signals.

4. A port independent data transaction interface as recited in claim 1, wherein the command channel further receives length data indicating a size of data corresponding to the command data, wherein the length data can indicate an arbitrary data size.

5. A port independent data transaction interface as recited in claim 4, wherein the command channel further receives address data indicating an address associated with data corresponding to the command data, wherein the address data can indicate an arbitrary starting location.

6. A port independent data transaction interface as recited in claim 1, wherein the command channel further receives a priority value indicating a priority level of the command data.

7. A port independent data transaction interface as recited in claim 6, wherein command data is processed based on an associated priority value.

8. A multi-port memory controller having port independent data transaction interface, comprising:

a command transfer storage that receives command data and a source id, the source id indicating a source device that transmitted the command data;

a data-in transfer storage that receives write data and a write source id, the write source id indicating a source device that transmitted the write data; and

a data-out transfer storage that provides read data and a read id, the read id indicating a source device that transmitted a read command corresponding to the read data.

9. A multi-port memory controller as recited in claim 8, wherein the source id is utilized to associate command data with corresponding write data.

10. A multi-port memory controller as recited in claim 9, wherein the write data transmitted to the data-in transfer storage and corresponding command data transmitted to the command transfer storage are processed when transmitted during different clock signals.

11. A multi-port memory controller as recited in claim 8, further including a separate data-in signal for each source device coupled to the multi-port memory controller.

12. A multi-port memory controller as recited in claim 11, wherein each data-in signal is coupled to the data-in transfer storage.

13. A multi-port memory controller as recited in claim 12, wherein each data-in signal further is coupled to a data path that circumvents the data-in transfer storage.

14. A multi-port memory controller as recited in claim 8, wherein the command transfer storage further receives a priority value indicating a priority level of the command data.

15. A multi-port memory controller as recited in claim 14, wherein command data is processed based on an associated priority value.

16. A method for performing data transactions in a multi-port system, comprising the operations of:

receiving command data and a source id on a command channel during a first clock cycle, the source id indicating a source device that transmitted the command data;

receiving write data and a write source id on a data-in channel during a second clock cycle, the write source id indicating a source device that transmitted the write data;

associating the command data with the write data based on the source id and the write source id; and

transmitting both the command data and write data to a processing circuit for further processing during a third clock cycle.

17. A method as recited in claim 16, wherein the first clock cycle, second clock cycle, and third clock cycle are each separated by a plurality of clock cycles.

18. A method as recited in claim 16, further comprising the operation of providing read data and a read id on a data-out channel during a fourth clock cycle, the read id indicating a source device that transmitted a read command corresponding to the read data.

19. A method as recited in claim 18, further comprising the operation of associating command data with the read data based on a source id and the read id.

20. A method as recited in claim 16, further comprising the operation of receiving a priority value on the command channel during the first clock cycle, wherein command data is processed based on an associated priority value.